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Parylene-C and High-k Polymer Bilayer Gate Dielectric for Low-Operating Voltage Organic Field-Effect Transistors

Tomoyuki Ashimine [a], Tomoaki Onoue [b], Takeshi Yasuda [c], Katsuhiko Fujita [c] & Tetsuo Tsutsui [c]

[a] Department of Applied Sciences for Electronics and Materials, Graduate School of Engineering Sciences, Kyushu University, Fukuoka, Japan

[b] Murata Manufacturing Co., Ltd., Kyoto, Japan

[c] Institute for Materials Chemistry and Engineering, Kyushu University, Fukuoka, Japan

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Parylene-C and High-*k* Polymer Bilayer Gate Dielectric for Low-Operating Voltage Organic Field-Effect Transistors

Tomoyuki Ashimine
Department of Applied Sciences for Electronics and Materials, Graduate School of Engineering Sciences, Kyushu University, Fukuoka, Japan

Tomoaki Onoue
Murata Manufacturing Co., Ltd., Kyoto, Japan

Takeshi Yasuda
Katsuhiko Fujita
Tetsuo Tsutsui
Institute for Materials Chemistry and Engineering, Kyushu University, Fukuoka, Japan

We propose a way to fabricate polymer insulators with a high gate capacitance for low-operating voltage organic field-effect transistors (OFETs). The insulator consists of spin-coated cyanoethylpullulan as a high-k polymer and chemical vapor deposited parylene-C as a covering layer. Parylene-C layer is insoluble in a common organic solvent, so the dielectric system can be fabricated on a layer of solution processable organic semiconductors such as poly(9,9-dioctylfluorene-co-bithiophene) (F8T2). The OFET shows a field-effect mobility of $3.4 \times 10^{-3}\,cm^2/Vs$, *a threshold voltage of* $-1\,V$, *and an on/off current ratio of* 5.9×10^2. *We successfully observed low-voltage operation in OFETs with this dielectric system.*

Keywords: chemical vapor deposition; gate dielectric; high-*k* polymer; organic field-effect transistors; parylene-C

INTRODUCTION

High-performance organic field-effect transistors (OFETs) are key to the development of flexible electronic devices such as low-end display driving circuits, low-cost memory devices and radio-frequency

Address correspondence to Takeshi Yasuda, Institute for Materials Chemistry and Engineering, Kyushu University, Kasuga, Fukuoka 816-8580, Japan. E-mail: yasuda@asem.kyushu-u.ac.jp

identification tags [1–2]. For optimal OFET performances, the dielectric materials used as insulator layers in OFETs should be carefully chosen because the characteristics of OFETs are significantly affected by interfacial properties of the dielectric. From this viewpoint, various polymer materials, such as polyimide, poly-4-vinylphenol (PVP) and poly-*p*-xylylene derivatives, have been examined for use as dielectric layers of OFETs [3]. Some devices using these polymers showed a higher mobility than those using silicon dioxide dielectrics. However their dielectric constants are rather small, so high operating voltages are required, often up to 100 V that is too high for practical application in general. Though there are some reports that fabricate low-operating voltage OFETs using inorganic high-k materials such as TiO_2, YO_X and CeO_2-SiO_2 for dielectric layers [4–6], insulators with a high dielectric constant should be produced from a soft organic material rather than a stiff inorganic material for flexibility or low-cost process. In this study, we fabricated Parylene-C and high-k polymer bilayer gate dielectric for low-operating voltage OFETs. These OFETs operated with supply voltages of less than -20 V. This result will increase the prospects of using OFETs in low-power applications.

EXPERIMENTAL

In this study, we fabricated the two kinds of OFET shown in Figure 1. For a bottom-gate configuration, a clean glass was used as a substrate and gold was sputtered through a shadow mask to form a 5 mm-wide and 30 nm-thick line as a gate electrode. For a high-k polymer layer, films with a thickness ranging from 1000 to 1300 nm of cyanoethylpullulan (CyEPL; $k = 18.6$ at 1 kHz) [7–9], as depicted in Figure 2, were prepared by spin-coating from 15 wt% solutions in dimethylformamide/acetone (9/1, w/w) at a spin rate of 3000 RPM. The poly-chloro-*p*-xylylene (Parylene-C; $k = 3.2$ at 1 kHz) [10] (Fig. 2) as a covering layer [11] was deposited subsequently by chemical vapor deposition with thickness ranging from 200 to 300 nm. The thickness was determined using a Sloan Dektak 3 profilometer. Organic semiconductor, 1,4-bis(4-methylstyryl)benzene (CH_3-OPV) (Fig. 2) [12] was purchased from Tokyo Chemical Industry Co. Ltd., and purified by train sublimation before use. The films with thickness ranging from 40 to 50 nm were vacuum-evaporated at below 2×10^{-6} Torr (deposition rate 0.05 nm/s) onto the dielectric layer at room temperature. Gold source-drain electrodes (40 nm) with an interdigitated configuration were deposited through a shadow mask. The channel length L and width W were 75 μm and 5 mm, respectively.

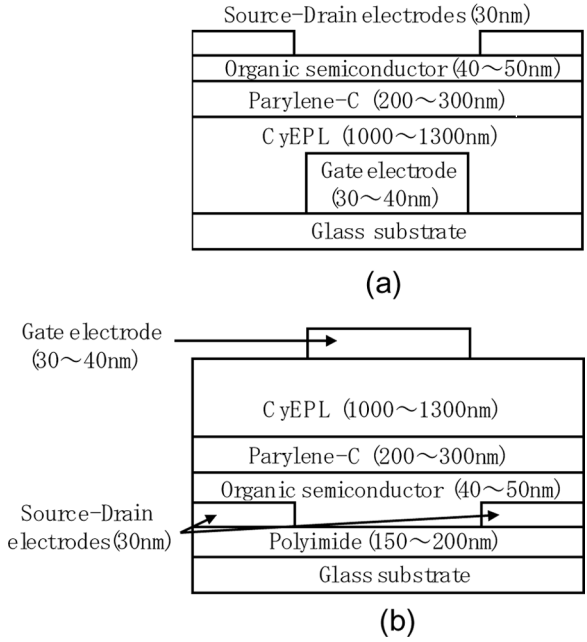

FIGURE 1 Schematic cross sections of the organic thin-film transistors, (a) bottom-gate configuration and (b) top-gate configuration.

For a top-gate configuration, clean glass substrates were spin-coated with a polyamic acid precursor solution and then baked at 300°C for 1 h to achieve full imidization. Gold source-drain electrodes with an interdigitated configuration were deposited through a shadow mask. Films with a thickness ranging from 40 to 60 nm of Poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2) purchased from American Dye Source, as depicted in Figure 2, were prepared by spin-coating from 0.5 wt% solutions in chloroform at a spin rate of 1500 RPM. In the next step, Parylene-C and CyEPL were deposited in sequence by the same way. Finally a gold gate electrode was spattered through a shadow mask.

The gate capacitances (C_i) of the device measured using a Solartron impedance analyzer system 1260/96. All devices were temporarily exposed to air prior to the measurement, and characterized using Agilent 4156C Precision Semiconductor Parameter Analyzer in a vacuum atmosphere. The electric parameters were estimated using a standard analytic theory of MOSFET according to the

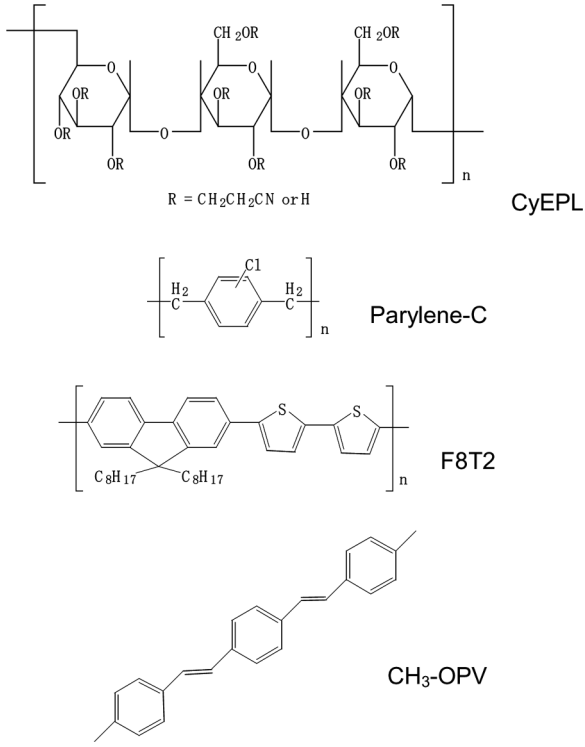

FIGURE 2 Molecular structures of cyanoethylpullulan (CyEPL), poly-chloro-*p*-xylylene (parylene-C), poly(9,9-dioctylfluorene-*co*-bithiophene) (F8T2) and 1,4-bis(4-methylstyryl)benzene (CH_3-OPV).

following equation:

$$I_{D,sat} = \frac{WC_i}{2L}\mu(V_G - V_T)^2$$

where $I_{D,sat}$ is the saturation drain current, C_i is the capacitance per unit area of the insulating layer, V_T is the threshold voltage, V_G is the gate voltage and μ is the field-effect mobility.

RESULTS AND DISCUSSION

We have recently reported the fabrication of OFETs using CH_3-OPV as a semiconductor and Parylene-C as a dielectric layer. CH_3-OPV gave the films with densely-packed submicron-size grains with a high degree of molecular order and the high field-effect hole mobility of

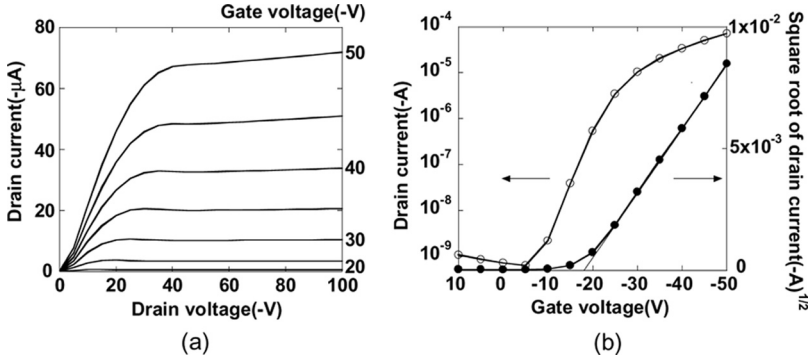

FIGURE 3 (a) Output characteristics and (b) transfer characteristics of CH_3-OPV-based OFET.

$0.13\,cm^2\,V^{-1}\,s^{-1}$ emerged with high on/off ratio of 5.8×10^5 [12]. However, high operating voltages are required, often exceeding $-40\,V$, which is too high for practical application in general. The performance increase of OFETs will be essential. The key to low voltage operation is reduction of the threshold voltage. Figure 3(a) shows the drain current (I_D) versus the drain voltage (V_D) with varying the applied gate voltage (V_G) and for bottom-gate OFETs using CH_3-OPV as a semiconductor and Parylene-C/CyEPL bilayer as a gate dielectric. From the transfer characteristics in Figure 3(b), the on/off drain current ratio ($V_D = -100$) was estimated to be 1.1×10^5. The device was found to have a field-effect mobility of $4.1 \times 10^{-1}\,cm^2/Vs$, a threshold voltage of $-18\,V$ and C_i of $9.4\,nF/cm^2$ (at 1 kHz). The obtained threshold voltage of the OFET was three times lower than that of the Parylene-C single-layer dielectric (C_i of $2.0\,nF/cm^2$). Table 1 compares the parameter of this stacked insulator and Parylene-C insulator for CH_3-OPV-based OFET. The device with single-layer dielectric using a spin-coated cyanoethylpullulan shows no stable saturation current, because of its gate leakage current due to ionic impurities.

TABLE 1 Characteristics of CH_3-OPV-based OFETs

	Parylene-C	Parylene-C + CyEPL
Mobility (cm^2/Vs)	1.8×10^{-1}	4.1×10^{-1}
On/off ratio	3.5×10^5	1.1×10^5
Threshold voltage (V)	-59	-18

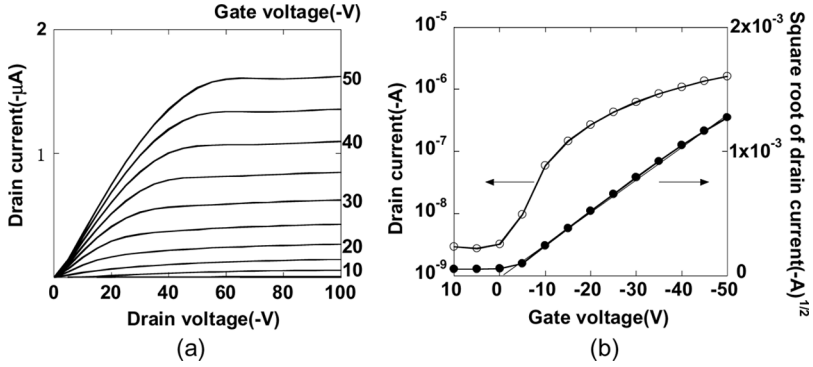

FIGURE 4 (a) Output characteristics and (b) transfer characteristics of F8T2-based OFET.

Since a vacuum-evaporated Parylene-C film could be deposited on any organic semiconductors, we tried to top-gate OFETs (insulator on organic semiconductor) in addition to bottom-gate OFETs. Figure 4(a) shows the drain current (I_D) versus the drain voltage (V_D) with varying the applied gate voltage (V_G) and for top-gate OFETs using F8T2 as a semiconductor and Parylene-C/CyEPL bilayer as a gate dielectric. From the transfer characteristics in Figure 4(b), the on/off off drain current ratio ($V_D = -100$) was estimated to be 5.9×10^2. The device was found to have a field-effect mobility of $3.4 \times 10^{-3}\,\mathrm{cm}^2/\mathrm{Vs}$, a threshold voltage of $-1\,\mathrm{V}$ and C_i of $7.1\,\mathrm{nF/cm}^2$ (at 1 kHz). Table 2 compares the parameter of this stacked insulator and parylene-C insulator for F8T2-based OFET. The obtained threshold voltage of the OFET was much lower than that of the Parylene-C single-layer dielectric. The device with single-layer dielectric using a spin-coated cyanoethylpullulan on the F8T2 layer shows no stable saturation current. The reason is assumed that CyEPL and F8T2 are soluble in many organic solvents, so that the interface of the semiconductor layer and insulating layer may be mixed when CyEPL is spin-coated directly on the F8T2 layer. Insertion of an insoluble Parylene-C layer between CyEPL

TABLE 2 Characteristics of F8T2-based OFETs

	Parylene-C	Parylene-C + CyEPL
Mobility ($\mathrm{cm}^2/\mathrm{Vs}$)	9.4×10^{-3}	3.4×10^{-3}
On/off ratio	5.1×10^4	5.1×10^2
Threshold voltage(V)	-19	-1

and F8T2 enables us to avoid the intermixing of layers. Thus the bilayer gate dielectric system can be also fabricated on a layer of solution processable polymeric semiconductors.

CONCLUSION

In summary, by using Parylene-C coated CyEPL as an effective gate dielectric, we were observing low-operating voltage OFETs characteristics. The function of the Parylrene-C coating layer might be to prevent ionic impurities in CyEPL from contact with the channel region; as a result, leakage current decreased in the stacked structure. We have also demonstrated that the palylene-C coating method also enables us to use a broad range of available polymeric semiconductors.

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